TTL Circuit - Transistor Transistor logic

It is a saturated logic. This circuit uses multiple-emitter transistor at the input. The number of emitters is equal to the desired fan-in of the circuit. A multi-emitter transistor is smaller in area the yield from a wafer is increased. Smaller area results in a lower capacitance to the substrate, reducing circuit ~~are~~ rise and fall times and hence increasing its speed

Basic circuit →

The basic circuit of the TTL family is the NAND gate

Circuit operation → If both inputs A & B are high (logic 1) then T1 has no emitter current, but its base collector junction is forward biased and

Therefore it will supply Friday case current to T_2 which feeds base current to T_1 causing it to conduct and output come.

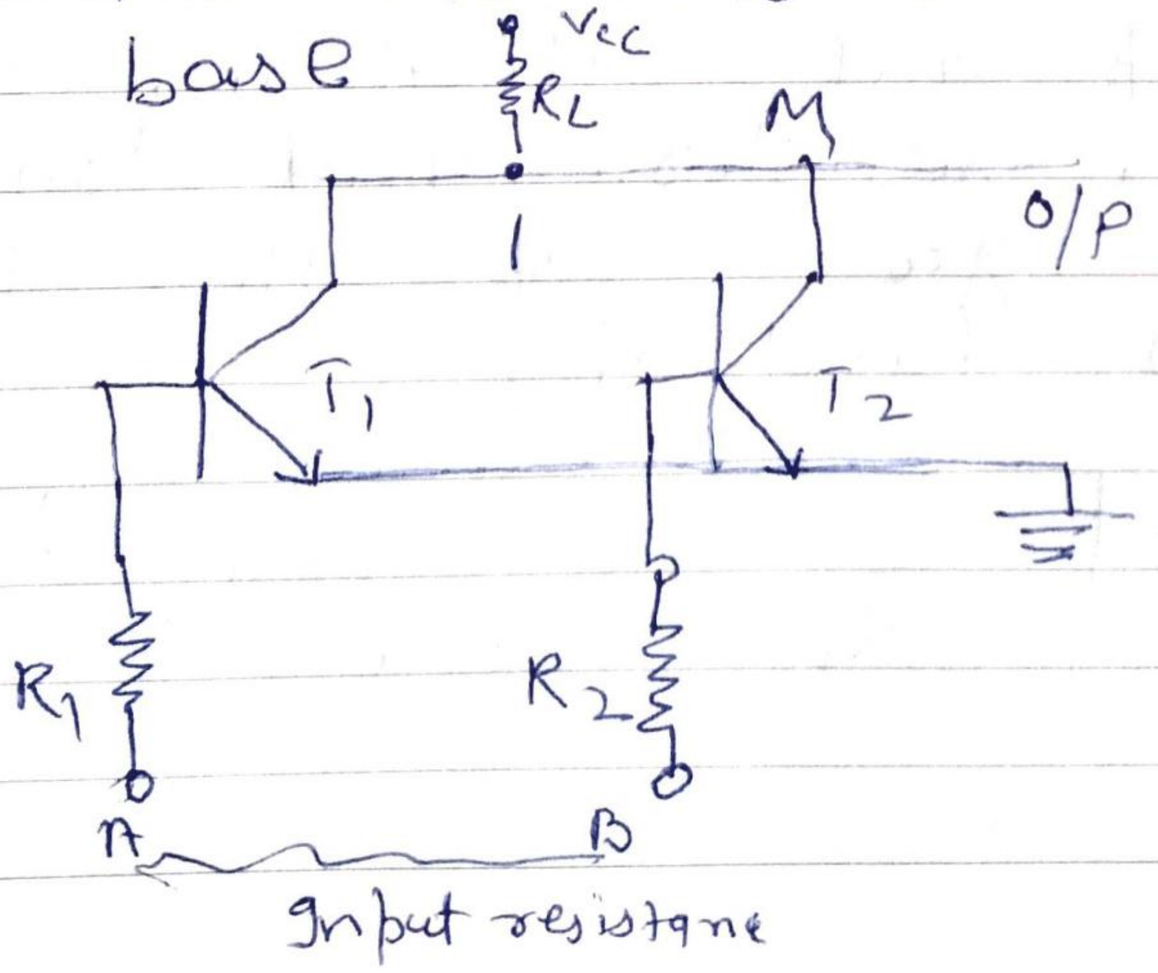
(logical 0) If either A or B goes low, then T_1 will have base emitter current placing T_2 to ground and thus T_2 is cut off. consequently, collector of T_2 will go high and cause $\overline{T_2}$ to conduct and,

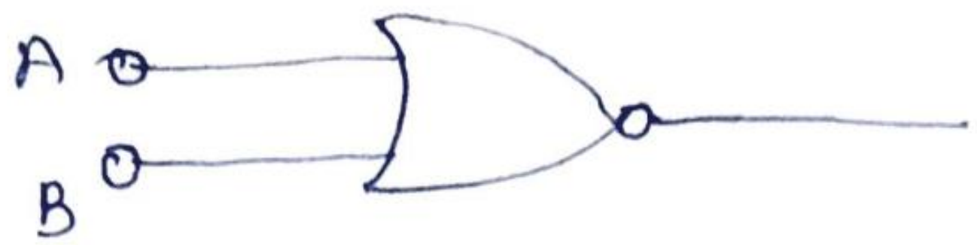
Thus we get an output in both cases.

Advances → The multible - emitter transistor replaces combinations of diodes, resistors and transistors found in other logic circuits. Thus its geometrical size is small, smaller size yields lower costs or more functions or both per given IC chip. It has high operating speed and high fan out.

(9.) RTL → Resistance - transistor logic

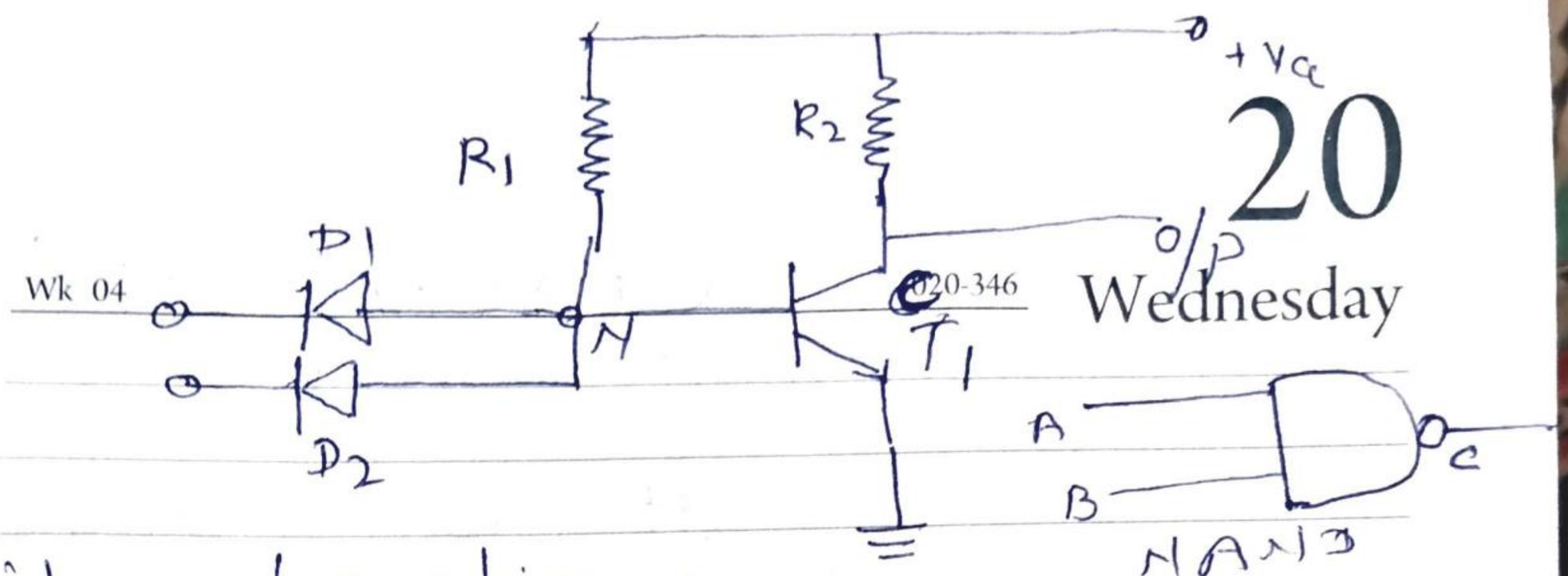
It is saturated logic. It uses only transistors and resistors as circuit elements and resistors in the input to each base





This family is based on the NOR circuit
Circuit operation → when both inputs A & B are 0V (ground), both transistors are turned OFF, hence point M goes to $+V_{cc}$ so that output in logic 1.
If either or both input terminals are at $+V_{cc}$ ie are high (or logic 1), one or both transistors would be fully turned ON (ie the voltage of point N to be 0V. Hence, output would be at logic 0.
RTL family has following characteristics
(1) relatively slow speed.
(2) low fan-out of 6 and a fan-in of 4.
(3) poor noise immunity.
(4) expensive
(5) cannot operate at speeds above 4 MHz.
(6) poor noise-immunity
Advantages → low power dissipation.

(Diode-Transistor-logic)
(2) DTL → It is a saturated logic because transistors operate between cut off and saturation. It consists of diodes, resistors and transistors. The basic gate of this family performs HAND function. The circuit basically consists of a diode AND gate followed by a transistors inverter which leads to a NAND gate



Circuit operation →
when both diode D1 & D2 have positive voltages applied to them (logic 1) neigher conducts and Trasistor T is ON by the current provided by Vcc through R_1. since trasistor T becomes saturated, point c is brought to 0V (logic 0). Hence, output goes logic 0.
gt either or both inputs are at 0V (logic 0). the diode will conduct at diviting point N to ground. i.e 0V. Since there is no base voltage for trasitor T, gt will be cut off OFF. Thereby driving point c and hence output to Vcc i.e logic 1.
gt is seen that output is low only when all intuts are high. The condition for NAND gate.
Charcterised
1. relatively lower speed.
2. Comparatively better noise immunity.
3. Trasmission delay on 30 ns.
4. a fan-in of 8
5. a fan-out of 5.

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Flip-Flops

Que (1) what is a Flip-Flops ?

A Flip-Flops is a bistable multivibrator which has two stable states. (0, 1) Zero and one. It can store 1 bit of information in its output. It can be used to count binary numbers, or store them in 'registers'. It can perform various logic operations and it is the basic building block of the "shift register' used in multiplication. It also used as the basic memory element in digital computers.

Que (2) the R.S Flip. Flops

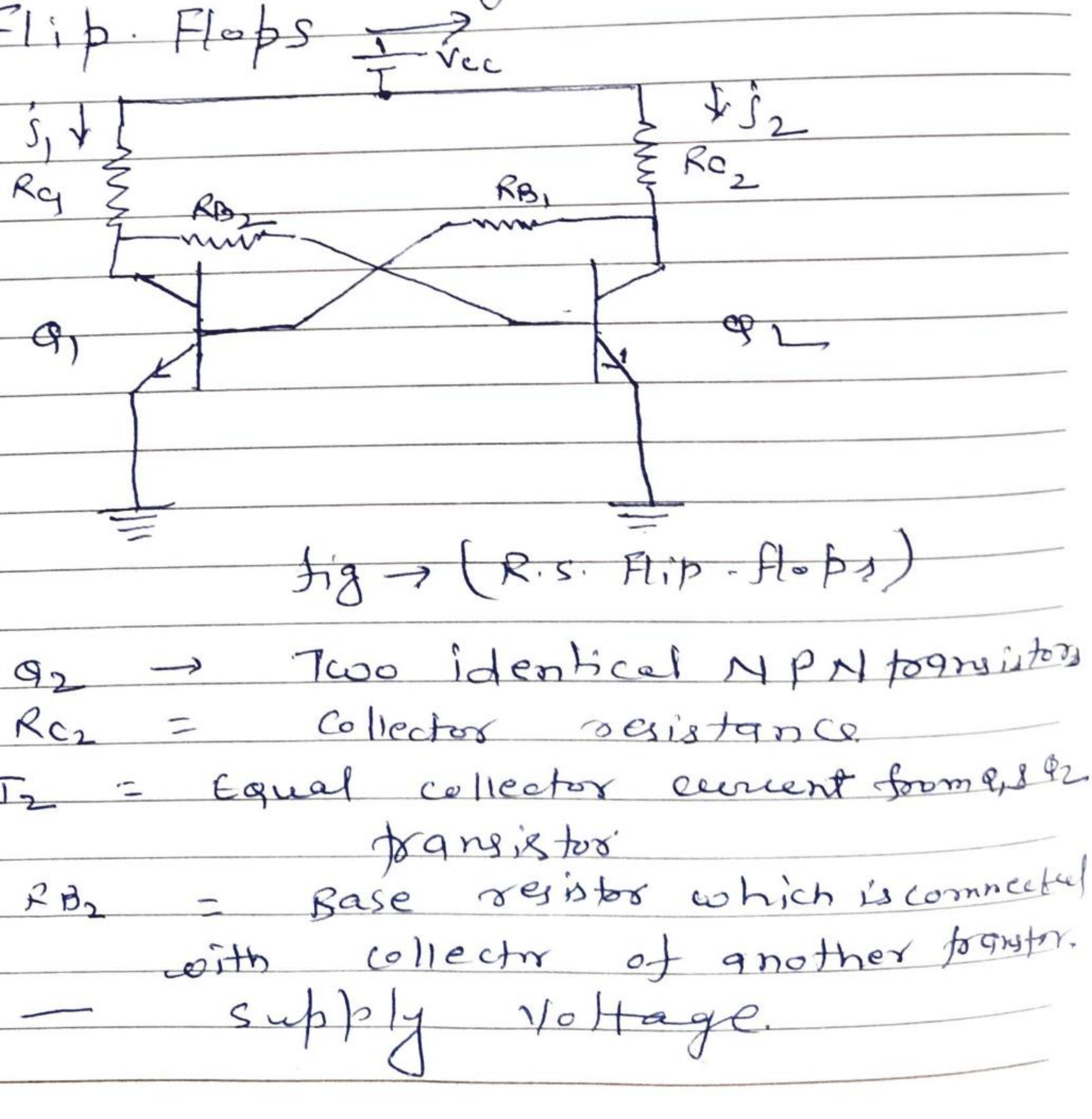

fig → (R.S. Flip-flops)

Q_1 & Q_2 → Two identical NPN transistors

R_{C_1} & R_{C_2} = Collector resistance.

I_1 & I_2 = Equal collector current from Q_1 & Q_2 transistor

R_{B_1} & R_{B_2} = Base resistor which is connected with collector of another transistor.

V_{CC} — supply voltage.

Circuit connection and operation →

Circuit consists of two identical common emitter (CE) amplifier stages with output of one fed to the input of the other by resistors RB_1 & RB_2. when Vcc is applied, one transistor will start conducting slightly ahead of the other due to some difference in the characteristics of the transistors. If Q_1 collector current (I_1) to increase, and so potential drop across the Q_1 collector resistance Rc_1 to increase and the positive collector voltage of transistor Q_1 to reduce. The rising collector voltage is coupled to the base of Q_2 through a resistance RB_1 where it forward biases the base-emitter Junction of Q_2. This will cause an increase in its collector current and decrease in collector voltage. The decreasing collector voltage is applied to the base of Q_1 where it further reverse biases the base emitter Junction of Q_1 to decrease its Collector current. with this set of action taking place, Q_2 is quickly driven to saturation and Q_1 to cut off. The circuit will now remain stable in this state until a negative trigger pulse at Q_2 changes this state.

If a small increase in the Q_2 collector current I_2, rather than in I_1

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the negative feedback action would have been in the opposite direction, i.e. the transistor Q_2 fully conducting and the transitor Q_1 being cutoff. Thus two stable state of a flip-flop, either the transistor Q_1 is ON, thus keeping the transistor Q_2 OFF, or the transistor Q_2 is ON, keeping the transistor Q_2 OFF.